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09/677,734	10/02/2000	Einar Hansson	1	3417

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EXAMINER	
KUMAR, PANKAJ	

ART UNIT	PAPER NUMBER
2631	4

DATE MAILED: 03/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/677,734	HANSSON, EINAR	
	Examiner	Art Unit	
	Pankaj Kumar	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 October 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The abstract of the disclosure is objected to because it needs to have between 50 and 150 words. Correction is required. See MPEP § 608.01(b).

Claim Objections

1. Claim 9 is objected to because of the following informalities: The period on line 9 of claim 1 should be removed. Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Claim 1 recites the limitation "said clock phases" in line 13. There is insufficient antecedent basis for this limitation in the claim.

5. Claim 13 recites the limitation "the clock phases" in line 11. There is insufficient antecedent basis for this limitation in the claim.

6. Claim 8 recites the limitation "and/or" which makes it indefinite as to what applicant regards as his invention.

7. Claims 2-12, 14-18 are rejected since they depend on rejected claim 1 or 13.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1, 2, 3, 5, 6, 8, 9, 10, 11, 13, 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Bergmann et al. 4,821,297.

10. As per claim 1, Bergmann teaches a clock and data recovery circuit comprising: a first data input (Bergmann fig. 1: data in;) receiving a data signal of a first frequency (Bergmann figs. 2, 3, 4: frequency indicated by the solid lines); a clock defining a timing signal of a second frequency (Bergmann figs. 2, 3, 4: vertical lines are the clock timing signal); a phase generator dividing a cycle of the timing signal into a number of N signal phases (Bergmann fig. 1: tapped delay line 14 dividing a clock into N phases; 16 with 14); a data sampling component sampling a portion of said data signal (Bergmann fig. 2, 3, 4: RD1 is a sample of a portion of the solid line data signal) causing a logic output statement based on a truth table (Bergmann col. 5: table; output of 20 in fig. 1), said data sampling component comprising a buffer component for buffering said data signal (Bergmann fig. 1: delay line and latches) and comprising a phase detector assigned to said buffer component (Bergmann fig. 1: 20 assigned to 18); a counter assigned to said phase detector (Bergmann col. 5 table: retimed data samples being counted through latches outputting RD1, RD2, RD3) with said logic output statement causing a reaction of said counter (Bergmann col. 5 table: hold, decrement, or increment); and a phase selector

assigned to said counter (Bergmann fig. 1: 22), wherein three or more of said clock phases are selected by said phase selector (Bergmann: Bergmann fig. 6: four phase selector outputs; over time as the system runs, 22 will be selecting many clock phases) and the data sampling is triggered by said three or more clock phases (Bergmann fig. 6: 36, 34, 32; fig. 1: one data in is being delayed three times to obtain three phase shifts of the data).

11. As per claim 2, Bergmann teaches a clock and data recovery circuit as claimed in claim 1, wherein said reaction of said counter is counting up, counting down, or holding of the counter with the counter value transferred to the phase selector assigned to select the clock phases (Bergmann col. 5 table: hold, decrement, or increment).

12. As per claim 3, Bergmann teaches a clock and data recovery circuit as claimed in claim 1, wherein the data signal is a binary signal having signal states zero or one defining a bit sequence (Bergmann cols. 3-4: "data bit").

13. As per claim 5, Bergmann teaches a clock and data recovery circuit as claimed in claim 1, wherein said buffer component comprises a first, a second and a third buffer portion each having a data input and a data output with the data inputs of the three buffer portions assigned to the first data input (Bergmann fig. 1: one data in into 12 producing 3 buffered or delayed data).

14. As per claim 6, Bergmann teaches a clock and data recovery circuit as claimed in claim 5, wherein said first, second and third buffer portions are triggered by a first clock phase I (Bergmann fig. 1: first delay in 12), a second clock phase j (Bergmann fig. 1: second delay in 12) and a third clock phase k (Bergmann fig. 1: third delay in 12), respectively, resulting in a buffering of the state of said data signal at said clock phases i, j and k (Bergmann fig. 1: output of 12 results in DD1, DD2, DD3).

15. As per claim 8, Bergmann teaches a clock and data recovery circuit as claimed in claim 6, further comprising a first output receiving the data signal from the buffer portion (Bergmann fig. 6: data out receiving data signal from buffers 36, 34, 32) which is triggered by the clock phase i and said data signal (Bergmann fig. 6: 36, 34, 32 triggered by data in and input from 38) and/or said timing signal is transmitted by said first output (Bergmann fig. 6: data out based on RD2 which is a signal based on time).

16. As per claim 9, Bergmann teaches a clock and data recovery circuit as claimed in one of claim 5, wherein the signal states of the data signal at the data outputs of said first, second and third buffer portions are detected by said phase detector (Bergmann fig. 1: 20).

17. As per claim 10, Bergmann teaches a clock and data recovery circuit as claimed in claim 9, wherein the phase detector further detects the signal state of the data signal (Bergmann fig. 1, col. 5 table shows signal state of data signal with RD1, RD2 and RD3) at the clock phase i (Bergmann fig. 1: output of 22) of the previous cycle of the timing signal (Bergmann fig. 1: three cycles of the timing signal as represented by DD1 or RD1, DD2 or RD2, DD3 or RD3 so anyone of the first two sets can be previous).

18. As per claim 11, Bergmann teaches a clock and data recovery circuit as claimed in claim 1, further comprising a low pass filter assigned to said phase detector (Bergmann paragraph 5: "a low pass filter to convert an error signal from the phase detector to an error voltage,").

19. As per claim 13, Bergmann teaches a method for clock and data recovery comprising: receiving a data signal of a first frequency (Bergmann figs. 2, 3, 4: frequency indicated by the solid lines); - defining a timing signal of a second frequency (Bergmann figs. 2, 3, 4: vertical lines are the clock timing signal); - dividing a cycle of the timing signal into a number of N

signal phases (Bergmann fig. 1: tapped delay line 14 dividing a clock into N phases; 16 with 14); sampling a portion of said data signal by a data sampling component (Bergmann fig. 2, 3, 4: RD1 is a sample of a portion of the solid line data signal) resulting in a binary number (Bergmann col. 5 has binary numbers for RD1), said data sampling component comprising a buffer component buffering said data signal and comprising a phase detector (Bergmann fig. 1: 12, 18, 20 buffer the data signal with 12, 18 as shown in fig. 3 and also has a phase detector in element 20); - looking up said binary number in a truth table yielding a logic output statement (Bergmann col. 5 shows binary numbers in the truth table which yields a logic output); and transmitting said logic output statement to a counter (Bergmann col. 5 table: retimed data samples being counted through latches outputting RD1, RD2, RD3) causing a reaction of said counter (Bergmann col. 5 table: hold, decrement, or increment) wherein the phase selector selects three or more of the clock phases (Bergmann fig. 6: four phase selector outputs; over time as the system runs, 22 will be selecting many clock phases) and triggers the data sampling by said three or more clock phases (Bergmann fig. 6: 36, 34, 32; fig. 1: one data in is being delayed three times to obtain three phase shifts of the data).

20. As per claim 14, Bergmann teaches a method as claimed in claim 13, wherein said counter is counting up, counting down, or holding the counter value as reaction on said logic output statement of the truth table (Bergmann col. 5: table has increment, decrement and hold) transferring the counter value to the phase selector assigned to select the clock phases (Bergmann fig. 1: output of 20 goes to 22; fig. 6: output of 20 goes to 38).

Claim Rejections - 35 USC § 103

21. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

22. Claims 4, 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bergmann in view of Stuart 3,746,800.

23. As per claim 4, Bergmann teaches a clock and data recovery circuit as claimed claim 1. What Bergmann does not teach is wherein said buffer component comprises bistable multivibrators. What Stuart teaches is wherein said buffer component comprises bistable multivibrators (Stuart fig. 7: flip flops 18, 20, 22, 24, 26, 28). It would have been obvious to one skilled in the art at the time of the invention to modify Bergmann with the bistable multivibrators in Stuart. One would be motivated to do so in order to control clock timing as taught by Stuart.

24. As per claim 12, Bergmann teaches a clock and data recovery circuit as claimed in claim 1. What Bergmann does not teach is dual rail amplifiers. What Stuart teaches is dual rail amplifiers (Stuart fig. 7: flip flops 18, 20, 22, 24, 26, 28). It would have been obvious to one skilled in the art at the time of the invention to modify Bergmann with the dual rail amplifiers in Stuart. One would be motivated to do so in order to control clock timing as taught by Stuart.

Allowable Subject Matter

25. Claims 7, 15, 16, 17, 18 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pankaj Kumar whose telephone number is (703) 305-0194. The examiner can normally be reached on Mon, Tues, Wed and Thurs after 8AM to after 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad H. Ghayour can be reached on (703) 306-3034. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PK

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PRIMARY EXAMINER